

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In Re Patent Application of:	)	
	)	
Benjamin S. Ting	)	Examiner: Le, Don P.
	)	
Application No.: Not yet assigned	)	Art Unit: 2819
	)	
Filed: Herewith	)	
	)	
For: ARCHITECTURE AND	)	
INTERCONNECT SCHEME FOR	)	
PROGRAMMABLE LOGIC	)	
CIRCUITS	)	
	)	
a Continuation of	)	
	)	
Application No. 10/269,364	)	
	)	
Filed: October 11, 2002	)	
	)	

Commissioner for Patents  
PO Box 1450  
Alexandria, Virginia 22313-1450

**INFORMATION DISCLOSURE STATEMENT**

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicants.

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Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

  X   37 C.F.R. §1.97(b).

       37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:

       A statement pursuant to 37 C.F.R. §1.97(e) or

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- (1) A statement pursuant to 37 C.F.R. §1.97(e); and
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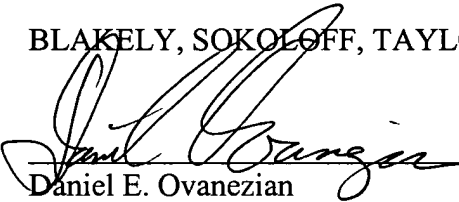
Pursuant to 37 C.F.R. § 1.98(d), no copies of cited art are enclosed. Prior art has been previously cited in parent application no. 10/269,364, filed October 11, 2002.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 10/23, 2003

  
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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 1207.P001C5	Application Number: Not yet assigned
	First Named Inventor: Benjamin S. Ting	
	Filing Date: Herewith	

### U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Code <sup>2</sup>	Kind (If known)			
		Re 34,363		Freeman	8/31/93	
		4,020,469		Manning	4/26/77	
		4,661,901		Veneski	4/28/87	
		4,700,187		Furtek	10/13/87	
		4,720,780		Dolecek	1/19/88	
		4,736,333		Mead, et al.	4/5/88	
		4,758,745		Elgamal	7/19/88	
		4,847,612		Kaplinsky	7/11/89	
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		4,912,342		Wong, et al.	3/27/90	

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		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (If known)				
		PCT	9208286			5/14/92		
		EPO	0415542			3/6/91		
		PCT	9410754			5/11/94		
		UK	2180382			3/25/87		

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<sup>1</sup>Unique citation designation number. <sup>2</sup>See attached Kinds of U.S. Patent Documents. <sup>3</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard S.3). <sup>4</sup>For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. <sup>5</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>6</sup>Applicant is to place a check mark here if English language Translation is attached.

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		4,918,440		Furtek	4/17/90	
		4,935,734		Austin	6/19/90	
		4,992,680		Benedetti, et al.	2/12/91	
		5,122,685		Chan et al.	6/92	
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		5,204,556		Shankar	4/20/93	
		5,208,491		Ebeling, et al.	5/4/93	
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		5,243,238		Kean	9/7/93	

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		5,260,610		Pederson, et al.	11/9/93	
		5,296,759		Sutherland, et al.	3/22/94	
		5,298,805		Garverick, et al.	3/29/94	
		5,329,470		Sample, et al.	7/12/94	
		5,396,126		Britton, et al.	3/7/95	
		5,457,410		Ting	10/10/95	

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		Number Code <sup>2</sup>	Kind  (If known)			
		5,469,003		Kean	11/21/95	
		5,477,067		Isomura, et al.	12/19/95	
		5,519,629		Snider	5/21/96	
		5,550,782		Cliff, et al.	8/27/96	
		5,581,767		Katuski, et al.	12/3/96	
		6,160,420		Gamal	12/12/00	

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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.:  001207.P001C5	Application Number:  Not yet assigned
Examiner: Le, Don P.		First Named Inventor: Benjamin S. Ting	
Art Unit: 2819 Confirmation No.: 2347		Filing Date: Herewith	

**OTHER ART - NO PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation <sup>2</sup>
		SPANDORFER, L.M., "Synthesis of Logic Functions on an Array of Integrated Circuits," Contract No. AF 19 (628) 2907, Project No. 4645, Task No. 464504, Final Report, November 30, 1965.	
		ATMEL Field Programmable Arrays, AT 6000 Series, 1993, p. 1-16.	
		Altera Corporation Data Sheet, Flex EPF81188 12,000 Gate Programmable Logic Device, September 1992, Ver. 1, pp. 1-20.	
		SHOUP, R. G., "Programmable Cellular Logic Arrays," Abstract, Ph.D. Dissertation, Carnegie Mellon University, Pittsburgh, PA, March 1970, (partial) pp. ii-121.	
		BRITTON, et al., "Optimized Reconfigurable Cell Array Architecture for High-Performance Field Programmable Gate Arrays," Proceedings of the IEEE 1993 Custom Integrated Circuits Conference, 1993, pp. 7.2.1. - 7.2.5.	
		BUFFOLI, E., et al., "Dynamically Reconfigurable Devices Used to Implement a Self-Tuning, High Performances PID Controller," 1989 IEEE, pp., 107-112.	
		DEVADES, S., et al., "Boolean Decomposition of Programmable Logic Arrays," IEEE 1988, pp. 2.5.1 - 2.5.5.	
		VIDAL, J. J., "Implementing Neural Nets with Programmable Logic," IEEE Transactions on Acoustic, Speech, and Signal Processing, Vol. 36, No. 7, July 1988, pp. 1180-1190.	
		LIU, D.L., et al., "Design of Large Embedded CMOS PLA's for Built-In Self-test," IEEE Transactions on Computed-Aided Design, Vol. 7, No. 1, January 1988, pp. 50-53.	
		SUN, Y., et al., "An Area Minimizer for Floorplans with L-Shaped Regions," 1992 International Conference on Computer Design, 1992 IEEE, pp. 383-386.	

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		Minnick, R.C., "A Survey of Microcellular Research", Vol. 14, No. 2, 4/1967, pp. 203-241.	
		Cliff, et al., "A Dual Granularity and Globally Interconnected Architecture for a Programmable Logic Device", IEEE '93 pp. 7.3.1-7.3.5.	
		Xilinx, "The Programmable Gate Array Data Book", 1992.	
		Wescon '93, pp. 321-326.	
		Wescon '93, pp. 310-320.	

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